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10/646,868	08/25/2003	Tatsuya Kawasaki	070639-0143	1667

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EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 08/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/646,868	KAWASAKI, TATSUYA	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *1-5* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. Applicant's request for reconsideration filed on 6/13/2006 has been reviewed.

2. Amendment filed on 6/13/2006 including amended claims (canceled claims 1-5, new claims 6-19) and amended drawings has been entered.

3. Applicant's arguments with respect to claims 6-19 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

4. Claim 6 is objected to because of the following informalities: In line 3 of claim 6, "a test circuit testing that tests" is incorrect. It should be --a test circuit that tests--. Appropriate correction is required.

5. Claim 15 is objected to because of the following informalities: In line 6 of claim 15, "memory circuit:" is incorrect. It should be –memory circuit;--. Appropriate correction is required.

6. Claim 19 is objected to because of the following informalities: In line 3 of claim 19, "test pattern register deceives" is incorrect. It should be --test pattern register receives--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 6, 7, 8, 12, 14, 18, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over So (US 5,883,844) in view of Akamatsu et al. (US 6,473,873 B1).

As per claim 6, So teaches a semiconductor device comprising: a memory circuit provided in a semiconductor substrate; and a test circuit testing that tests said memory circuit in a test mode and is incorporated into said semiconductor substrate together with said memory circuit, said test circuit comprising: an address register storing an address data (fig. 1, abstract, col. 1, lines 48-50, col. 2, lines 44-46, lines 54-56, col. 4, lines 32-33, So).

However So does not explicitly teach the specific use of a test pattern register storing a test pattern data, said test pattern data being written in said memory circuit in said test mode; said test pattern data being written in an address of said memory circuit indicated by said address data; and a fixed external terminal shared to receive serially said test pattern data and said address data.

Akamatsu et al. in an analogous art teach that a plurality of terminals...data input/output (fig. 11, col. 2, lines 48-56, Akamatsu et al.). Akamatsu et al. teach that FIG. 4 shows... test patterns (fig. 4, col. 7, lines 58-60, Akamatsu et al.). Akamatsu et al. teach that the shift register circuit...memory section WL (fig. 4, col. 8, lines 1-21, Akamatsu et al.). Akamatsu et al. teach that in the test mode...internal address signal (IAD_1 to IAD_n), (col. 11, line 53 to col. 12, line 5, Akamatsu et al.). Akamatsu et al. teach that input/output terminals...address signal (fig. 11, col. 14, lines 14-18, Akamatsu et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify So's patent with the teachings of Akamatsu et al. by including an additional step of using a test pattern register storing a test pattern data, said test pattern data being written in said memory circuit in said test mode; said test pattern data being written in an address of said memory circuit indicated by said address data; and a fixed external terminal shared to receive serially said test pattern data and said address data.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to reduce the number of terminals of the semiconductor memory device.

- As per claim 7, So and Akamatsu et al. teach additional limitations.

So teaches the semiconductor device wherein said test circuit further comprises: a selection register storing a selection data, said selection data indicating which of said test pattern register and said address register receives data from said first external terminal (col. 6, lines 14-18, So).

- As per claim 8, So and Akamatsu et al. teach additional limitations.

Akamatsu et al. teach the semiconductor device wherein said first external terminal is shared to receive serially said selection data (fig. 11, col. 14, lines 14-18, Akamatsu et al.).

- As per claim 12, So and Akamatsu et al. teach additional limitations.

Akamatsu et al. teach the semiconductor device, wherein said test mode has a test setting mode and a test executing mode, in said test setting mode, said test pattern register and said address register receive said test pattern data and said address data respectively, in said test executing mode, said test pattern register and said address register output data stored therein to said memory device, said test setting mode is conducted when a test control signal input from a second external terminal has one logic state, and said test executing mode is conducted when said test control signal has another logic state (fig. 10, col. 11, line 18 to col. 12, line 22, Akamatsu et al.).

- As per claim 14, So and Akamatsu et al. teach additional limitations.

Akamatsu et al. teach the semiconductor device, wherein said test pattern register and said address register are shift registers (col. 8, lines 1-4, Akamatsu et al.).

- As per claim 18, So and Akamatsu et al. teach additional limitations.

Akamatsu et al. teach the semiconductor device, further comprising a second external terminal receiving a setting mode data, wherein said test pattern register or said address register receives said test pattern data or said address data respectively from said first external terminal when said setting mode data has one logic state, and said selection register receives said selection data from said first external terminal when said setting mode data has another logic state (fig. 10, 11, col. 11, line 18 to col. 12, line 22, col. 14, lines 15-19, Akamatsu et al.).

- As per claim 19, So and Akamatsu et al. teach additional limitations.

Akamatsu et al. teach the semiconductor device, further comprising a second external terminal receiving a setting mode data, wherein said test pattern register receives said test pattern data from said first

external terminal, and said selection register receives said selection data from said first external terminal when said setting mode data has another logic state (fig. 10, 11, col. 11, line 18 to col. 12, line 22, col. 14, lines 15-19, Akamatsu et al.).

10. Claims 9, 10, 11, 16, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over So (US 5,883,844) and Akamatsu et al. (US 6,473,873 B1) as applied to claim 6 above, and further in view of Gittinger et al. (US 5,668,815).

As per claim 9, So and Akamatsu et al. substantially teach the claimed invention described in claim 6 (as rejected above).

However So and Akamatsu et al. do not explicitly teach the specific use of the semiconductor device wherein said test circuit further comprises: an addressing register storing an addressing mode data, said addressing mode data indicating how said memory circuit is addressed to write said test pattern data.

Gittinger et al. in an analogous art teach that the control register...memory or I/O space (col. 11, lines 46-61, Gittinger et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify So's patent with the teachings of Gittinger et al. by including an additional step of using the semiconductor device wherein said test circuit further comprises: an addressing register storing an addressing mode data, said addressing mode data indicating how said memory circuit is addressed to write said test pattern data.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to address the memory in different modes to write the test pattern data.

- As per claim 10, So, Akamatsu et al. and Gittinger et al. teach additional limitations.

Gittinger et al. teach the semiconductor device wherein said addressing mode data indicates whether said address data is incremented or decremented (col. 11, lines 46-61, Gittinger et al.).

- As per claim 11, So, Akamatsu et al. and Gittinger et al. teach additional limitations.

Gittinger et al. teach the semiconductor device wherein said first external terminal is shared to receive said addressing mode data (fig. 3, col. 9, lines 50-65, Gittinger et al.).

- As per claim 16, So, Akamatsu et al. and Gittinger et al. teach additional limitations.

Gittinger et al. teach the semiconductor device, wherein said test circuit further comprises an addressing register storing an addressing mode data, said addressing mode data indicating how said memory circuit is addressed to write said test pattern data (col. 11, lines 46-61, Gittinger et al.).

- As per claim 17, So, Akamatsu et al. and Gittinger et al. teach additional limitations.

Gittinger et al. teach the semiconductor device wherein said addressing mode data indicates whether said address data is incremented or decremented (col. 11, lines 46-61, Gittinger et al.).

11. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over So (US 5,883,844) and Akamatsu et al. (US 6,473,873 B1) as applied to claim 6 above, and further in view of Matshushita (JP 2002100200 A).

As per claim 13, So and Akamatsu et al. substantially teach the claimed invention described in claim 6 (as rejected above).

However So and Akamatsu et al. do not explicitly teach the specific use of the semiconductor device, wherein said test circuit further comprises a reverse circuit outputting data in which the value of said test pattern data is reversed.

Matshushita in an analogous art teaches a pattern reversal circuit (abstract, Matshushita).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify So's patent with the teachings of Matshushita by including an additional step of using the semiconductor device, wherein said test circuit further comprises a reverse circuit outputting data in which the value of said test pattern data is reversed.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to provide a different test pattern to test memory circuit.

12. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over So (US 5,883,844) in view of Akamatsu et al. (US 6,473,873 B1).

As per claim 15, So teaches a semiconductor device comprising: a memory circuit provided in a semiconductor substrate; and a test circuit that tests said memory circuit in a test mode and is

incorporated into said semiconductor substrate together with said memory circuit (fig. 1, abstract, col. 1, lines 48-50, col. 2, lines 44-46, lines 54-56, col. 4, lines 32-33, So), said test circuit comprising: a selection register storing a selection data, said selection data indicating whether said test pattern register is selected to receive said test pattern data (col. 6, lines 14-18, So).

However So does not explicitly teach the specific use of a test pattern register storing a test pattern data, said test pattern data being written in said memory circuit; and a first external terminal shared to receive serially said test pattern data and said selection data.

Akamatsu et al. in an analogous art teach that a plurality of terminals...data input/output (fig. 11, col. 2, lines 48-56, Akamatsu et al.). Akamatsu et al. teach that FIG. 4 shows... test patterns (fig. 4, col. 7, lines 58-60, Akamatsu et al.). Akamatsu et al. teach that the shift register circuit...memory section WL (fig. 4, col. 8, lines 1-21, Akamatsu et al.). Akamatsu et al. teach that in the test mode...internal address signal (IAD_1 to IAD_n), (col. 11, line 53 to col. 12, line 5, Akamatsu et al.). Akamatsu et al. teach that input/output terminals...address signal (fig. 11, col. 14, lines 14-18, Akamatsu et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify So's patent with the teachings of Akamatsu et al. by including an additional step of using a test pattern register storing a test pattern data, said test pattern data being written in said memory circuit; and a first external terminal shared to receive serially said test pattern data and said selection data.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to reduce the number of terminals of the semiconductor memory device.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH

shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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